Notice of Allowability	Application No.	Applicant(s)	
	10/050,793	EBINA, AKIHIKO	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment after final dated 2/17/04*.

2. ☒ The allowed claim(s) is/are *1-15*.

3. ☒ The drawings filed on *18 January 2002 and 25 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Minhloan Tran
Primary Examiner
Art Unit 2826

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

A. Claims 2-11 and 15 are allowed for the reasons given in papers mailed 05/22/2003 and 12/16/2003.

Claims 1 and 12-14 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a BiCMOS inverter having an insulation layer; a semiconductor layer formed on the insulation layer; an element isolation region formed in the semiconductor layer; and a first element forming region and a second element forming region defined by the element isolation region; wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor; the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type, the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type, the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type, the first body region of the second conduction type is electrically connected to the source region of the first conduction type, the first body region of the second conduction type is in contact with and thereby electrically con-

nected to the first base region of the second conduction type, the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor, the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type, the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type, the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type, the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type, the source region of the second conduction type is electrically connected to the second collector region of the first conduction type, the drain region of the second conduction type is electrically connected to the second base region of the second conduction type, the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and the first gate electrode layer is electrically connected to the second gate electrode layer, as recited in claim 1.

Hara et al. 5,126,595 discloses a BiCMOS inverter comprising a semiconductor layer, and first and second element forming regions 32; a first bi-polar transistor 28 and a first field effect transistor 23; the first bi-polar transistor 28 includes a first emitter region (**E1**) of a first conduction type, a first base region (**B1**) of a second conduction type, and a first collector region (**C1**) of the first conduction type, the first field effect transistor 23 includes a first gate electrode layer (**G1**), a source region (**S1**) of the first conduction type, and a drain region (**D1**) of the first conduction type, a second bi-polar transistor 25 and a second field effect transistor 22, the second bi-polar transistor 25 includes a second emitter region (**E2**) of the first conduction type, a second base region (**B2**) of the second conduction type, and a second collector region (**C2**) of the first conduction type, the second field effect transistor 22 includes a second gate electrode layer (**G2**), a source region (**S2**) of the second conduction type, and a drain region of the second conduction type, the first field effect transistor 23 further includes a first body region of the second conduction type (**1st body**, since it is in the 1st FET) formed at least between **S1** and **D1**, and the second field effect transistor 22 further including a first body region of the first conduction type (**2nd body**, since it is in the 2nd FET) formed at least between **S2** and **D2**, **G1** is electrically connected to **G2**, (G1 and G2 FORMING INPUT NODE 21), **D1** is electrically connected to **C1** which is electrically connected to **E2** (C1 AND E2 FORMING OUTPUT NODE 26), **S2** and the **2nd body** are electrically connected to **C2** at bus voltage (Vcc) connection 24, **D2** is electrically connected to **B2**, and **E1** is (ATTACHED TO GROUND

AT 29 AND) formed structurally isolated from **S1**, **S1** and the **1st body** being electrically connected to **B1**. Note figure 2 of Hara et al. Note that Hara et al. uses the older nomenclature of referring to the body of a MOSFET, when externally connected, as the "back gate." However, Hara et al. does not disclose or suggest or that the **1st body** is in contact with **B1** or the semiconductor layer is formed on an insulation layer (SOI), that the first and second element forming regions are defined by an element isolation region formed in the semiconductor layer, or that the first element forming region includes both the first bi-polar transistor and the first field effect transistor, or that the second element forming region includes both the second bi-polar transistor and the second field effect transistor. Note figure 3 of Hara et al. showing the absence of the insulation layer (SOI) and the element isolation region, and the fact that element forming elements 32 include only a single transistor, either MOSFET or bipolar but not both.

Tsuda et al. 6,246,104, recently cited by the applicant, discloses "a complementary BiCMOS circuit which comprises npn-type bipolar transistors 114 and 115, p-type MOS transistors 116 and 117 and n-type MOS transistors 118 and 119 ... formed on a silicon layer on an insulating film." Note column 10 lines 61-65 of Tsuda et al. Tsuda et al. elsewhere discloses an element isolation region 6 separating said silicon layer on said insulating film into multiple element forming regions. Note figure 1 of Tsuda et al. But neither Tsuda et al. nor Hara et al., alone or together, suggest or disclose the entire combination claimed in claim 1, especially the limitations that each of the two FETs be formed in the same ele-

ment isolation region with the one of the two BPTs to whose base the body, or back-gate, of that FET is tied, and that the base-body tie is direct (actual contact required) in the instance where the one of the complementary MOSFETs' body has the same conductivity type as the base of the BPTs (note that both BPTs have the same type).

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
03/2004